More than an Evolution: a New Power MOSFET Technology for Higher Efficiency of Power Supplies

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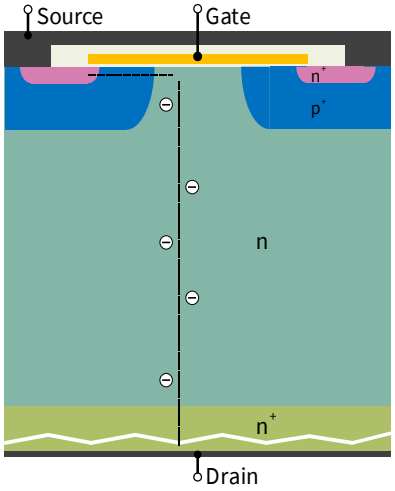
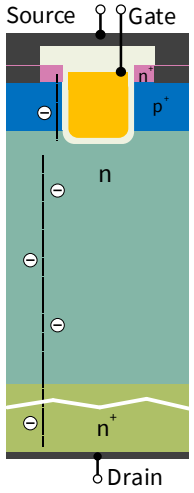
Evolution of vertical power MOSFET cell structures

Vertical DMOS
(~1980)



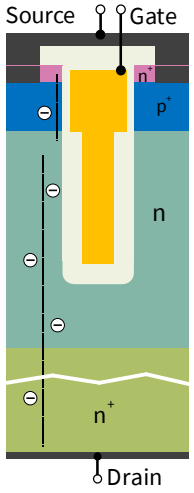
- Vertical current flow
- Strong impact of JFET pinch on $R_{DS(on)}$

Trench MOSFET
(~1992)



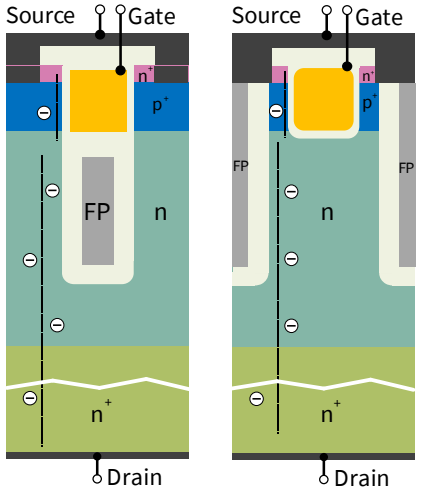
- Elimination of parasitic JFET
- Improves R_{on} x A

Field-plate MOSFET
(2001)



- Applies charge compensation
- Improves R_{on} x A and BV

Buried FP & Split-gate MOSFETs
(2002) (~2007)



- Separation of gate and field-plate
- Improves gate, gate-drain charges and FOM

NEXT
(now)

?

Outline

- The next level in Power MOSFET Technology Evolution
- Key performance indicators for fast-switching applications
- Application results: hard- and soft-switching DC/DC intermediate bus converters
- Conclusion

The next level in Power MOSFET Technology Evolution

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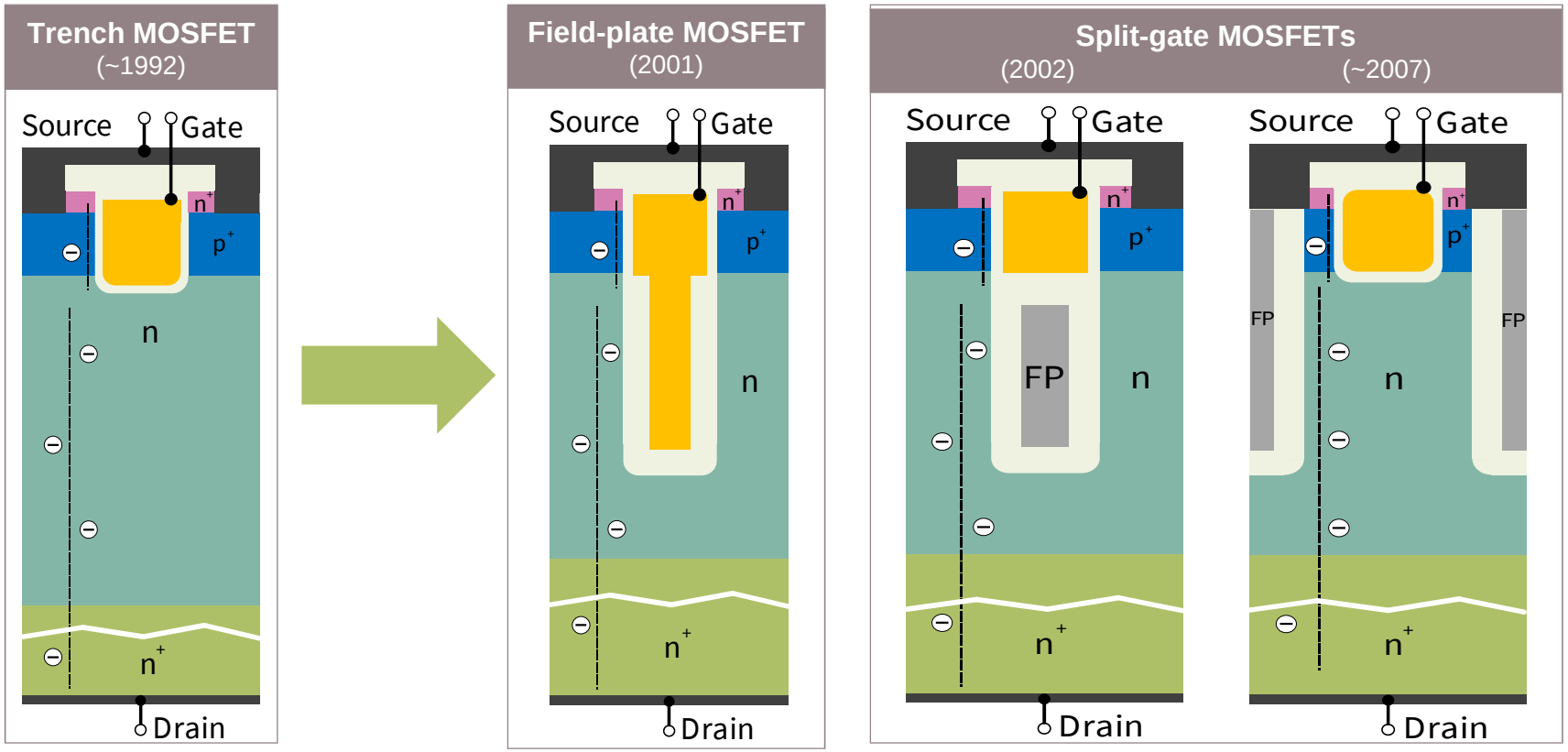
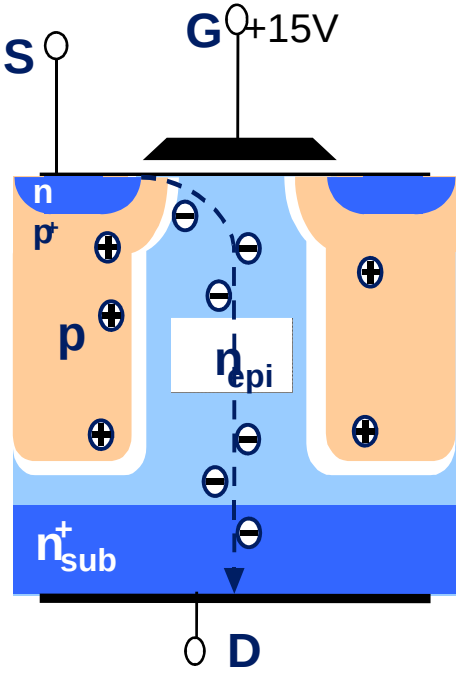
MOSFET structures based on charge compensation



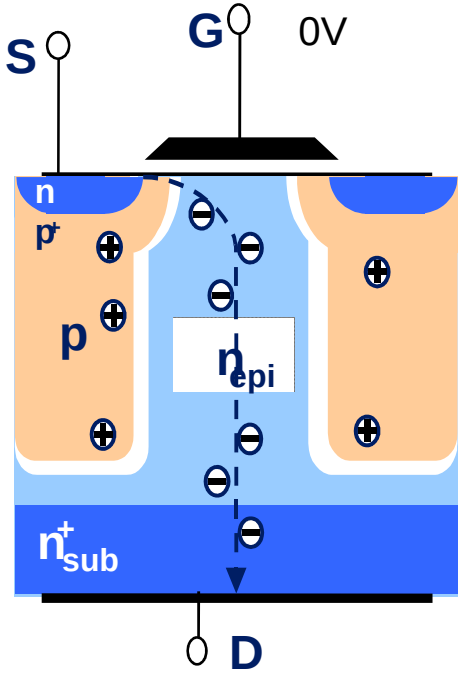
Basics of lateral charge compensation structures

– Several structures exist to overcome the unipolar silicon limit

On state



Heavy doping ensures low $R_{ds(on)}$ in on state

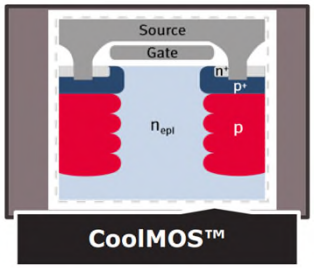


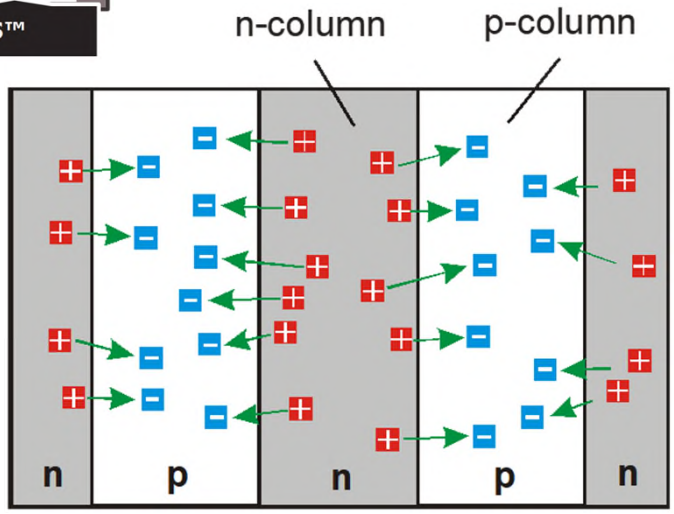
Off state

Compensation between holes in P column and electrons in epitaxial in off state

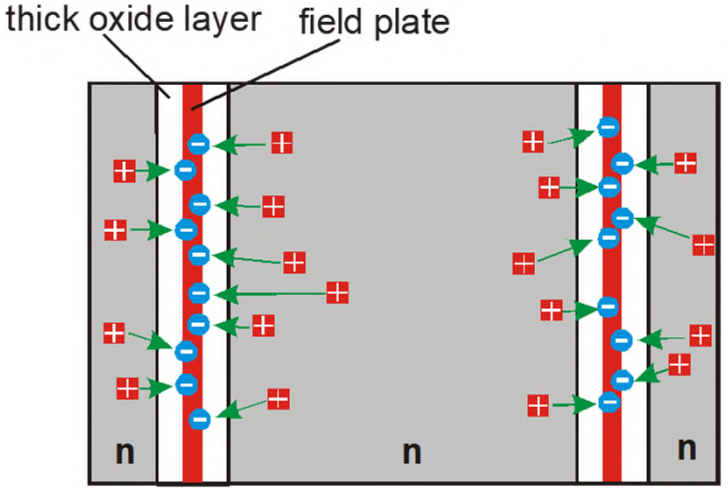
Basics of lateral charge compensation structures

- Super-junction devices are suited for larger blocking voltages
- Field-plate structures are advantageous for lower voltages

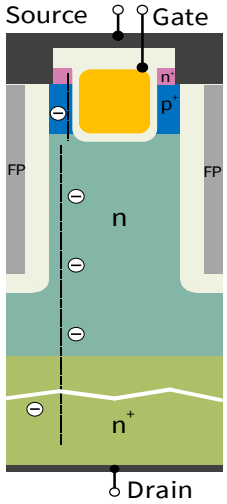




Compensation by p and n columns
(Super Junction)

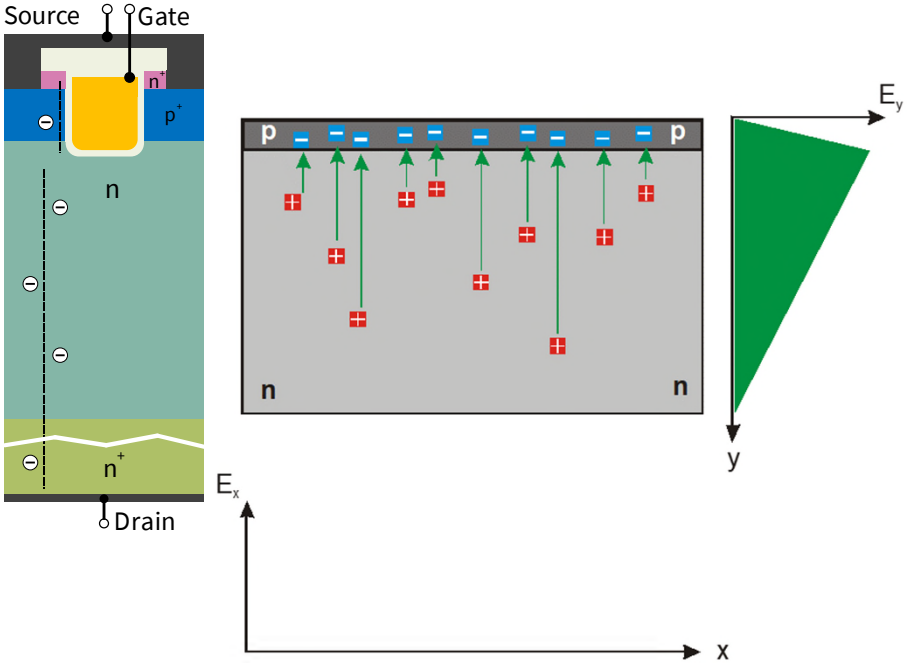


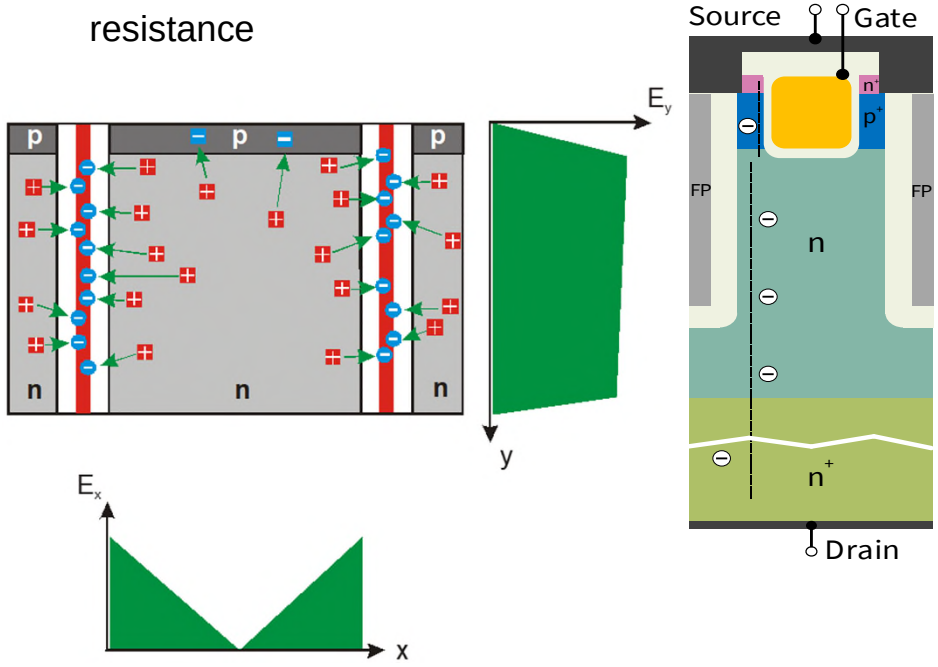
Compensation by field-plate



Electric Field Distribution

- 1D pn-junction
  - triangular-shaped field in vertical direction
- 2D charge compensation
  - trapezoidal-shaped field in vertical direction
  - triangular-shaped field in lateral direction
  - allows increased doping to reduce on-resistance





The next chapter in power MOSFET cell evolution

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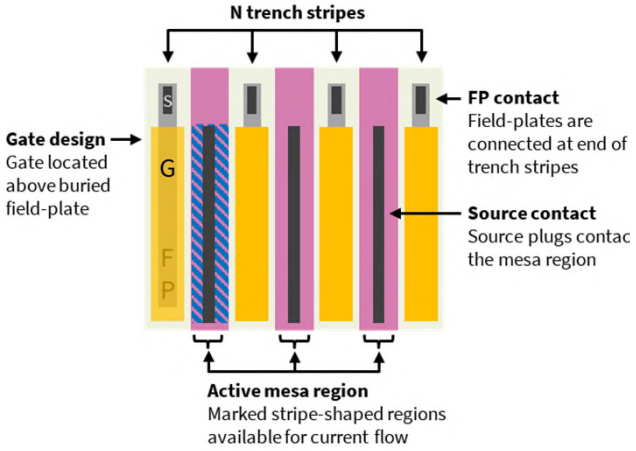
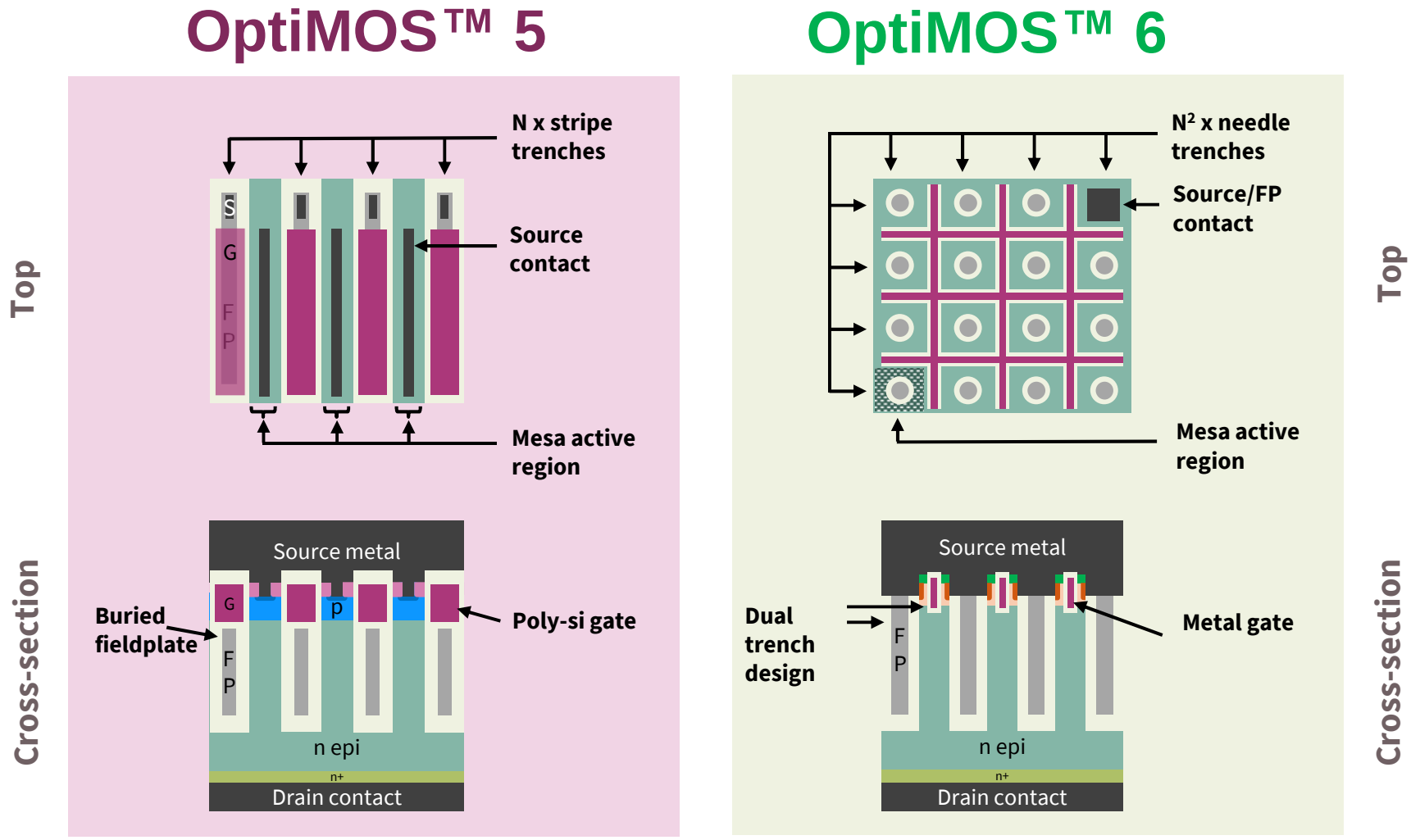
Industry‘s standard 2D stripe-trench cell concept

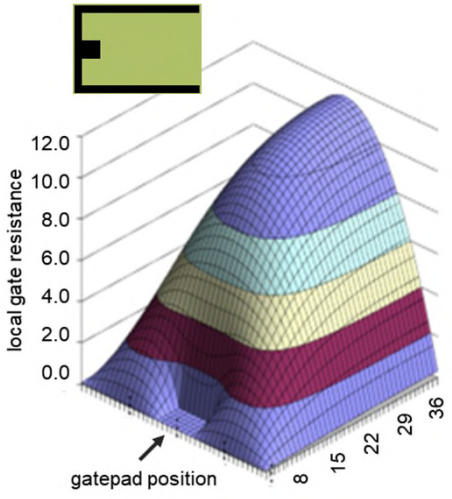


The next chapter in power MOSFET cell evolution



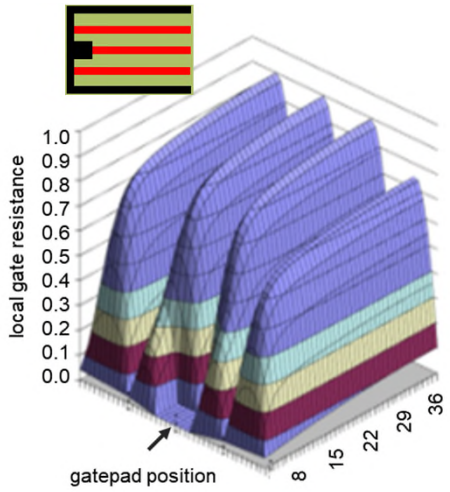
First trench power MOSFET technology with metal gate

Poly-silicon
0 gate fingers



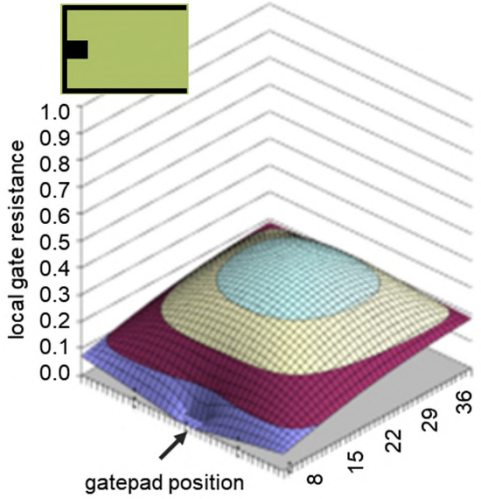
High value for equivalent gate resistance R_g

Poly-silicon
3 gate fingers



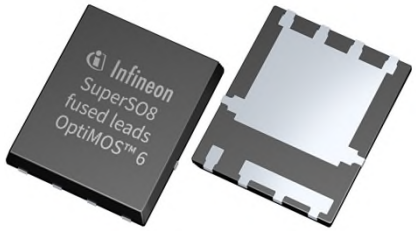
While gate fingers help to reduce the equivalent gate resistance, the distribution remains inhomogeneous, with relevant local deviations

Metal gate
No gate fingers needed



Using a metal gate yields a very homogeneous resistance over the chip, supporting fast switching

The benefit of using a metal gate



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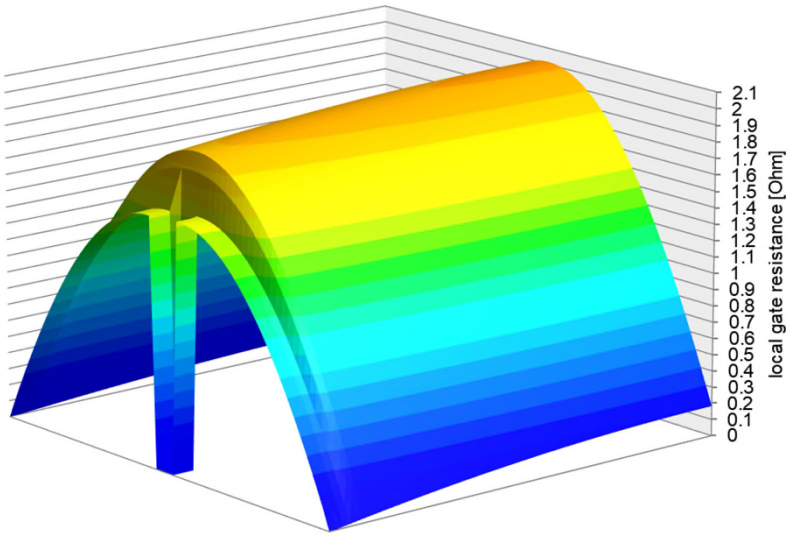
High value for equivalent gate resistance, can be improved with gate fingers on cost of area



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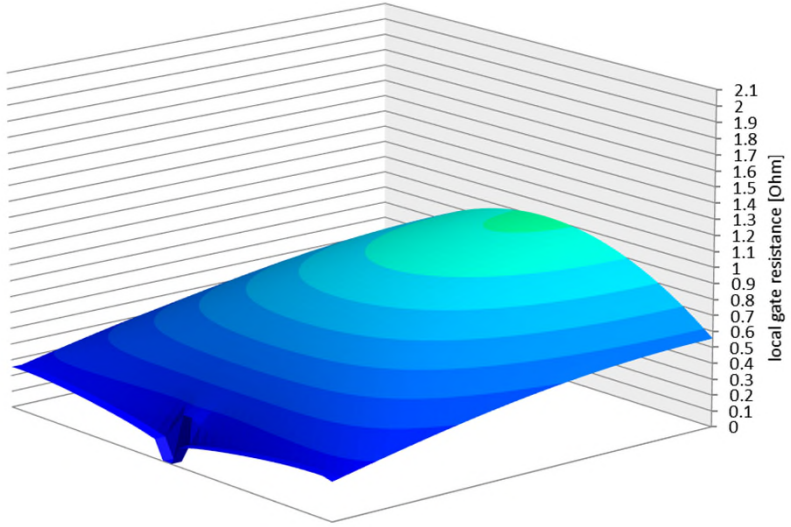
Using a metal gate yields a very homogeneous gate resistance over the chip, supporting fast switching



Distributed gate resistance for a common stripe design (left) and the new grid-like design (right)

Direct connection of field-plates with source metallization

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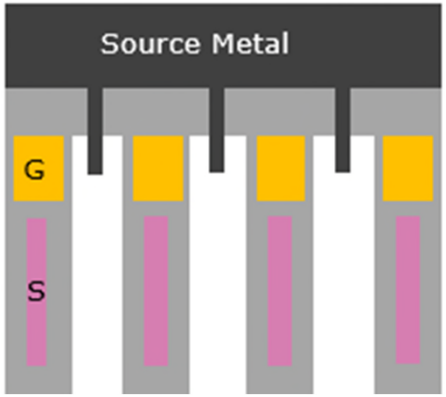
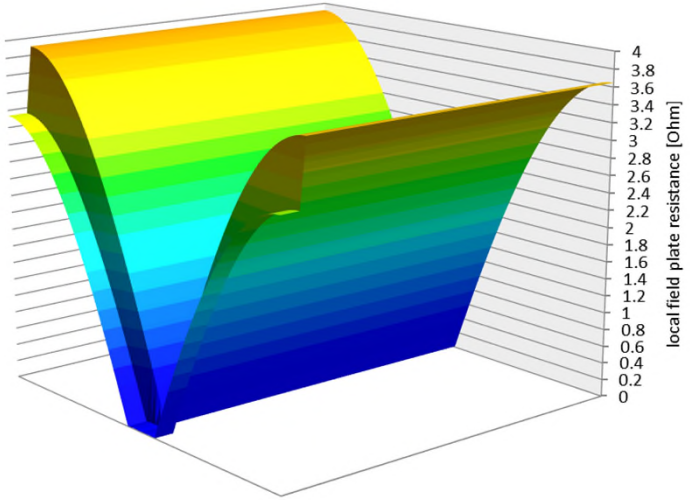
Significant variation of equivalent field-plate resistance, slows down switching speed





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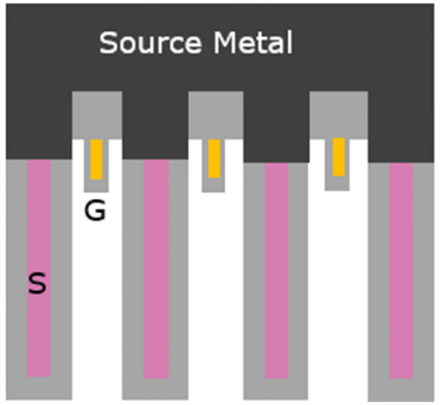
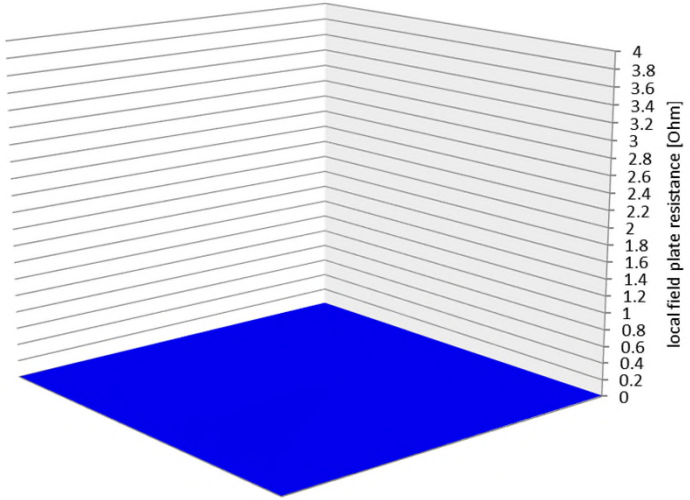
Direct connection of needle field-plates to source metallization practically eliminates field-plate resistance





Distributed field plate resistance for a common stripe design (left) and the new grid-like design (right)

Key performance indicators for fast-switching applications

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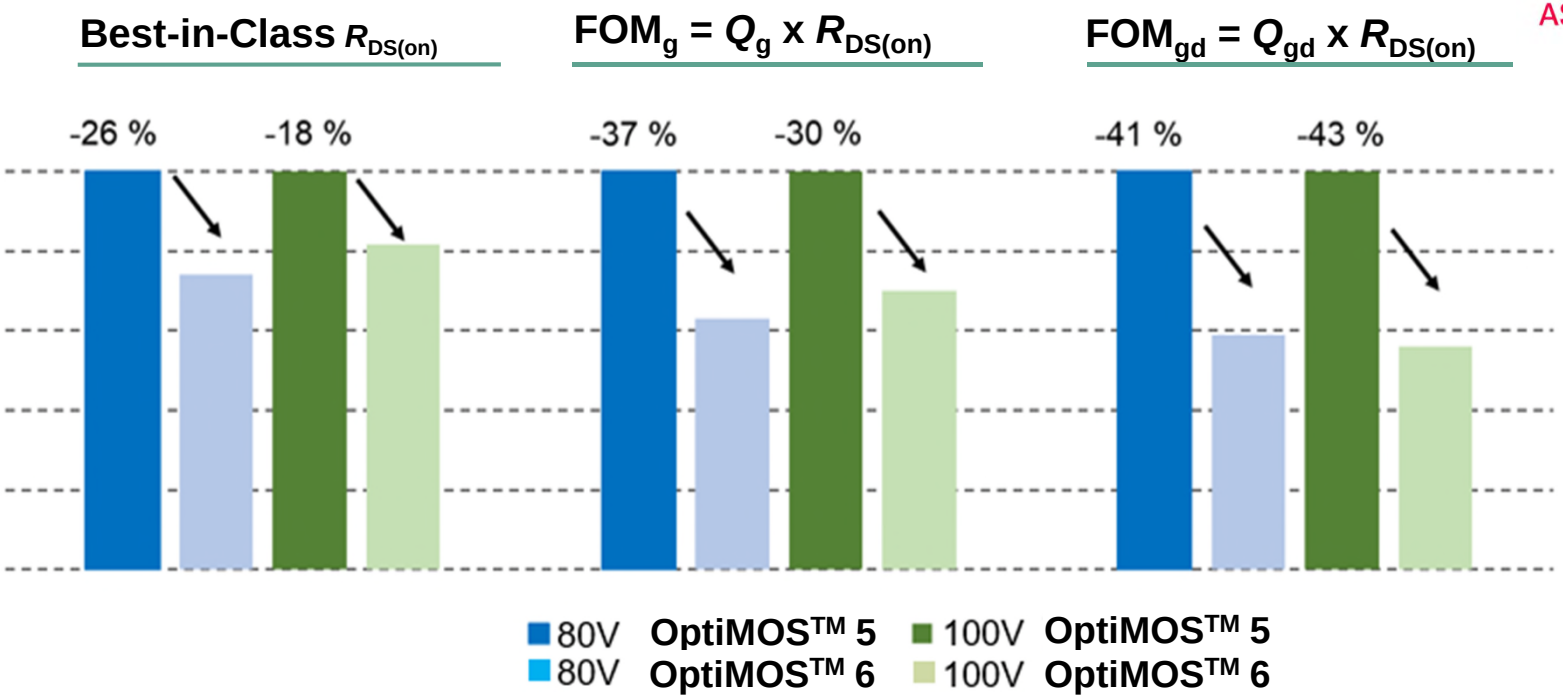
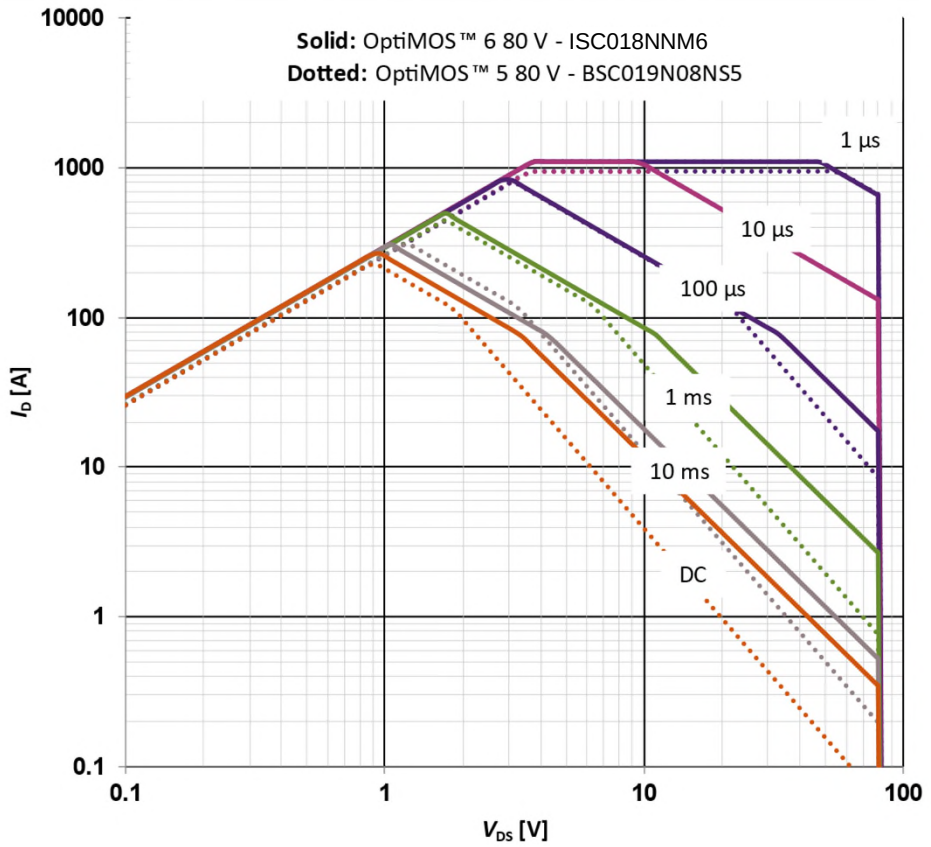
Figures of merit: specific on-resistance, FOMg and FOMgd



The **OptiMOS™ 6** improve $R_{DS(on)}$ besides carrying **low charges**, showing **industry's lowest** $R_{DS(on)}$ across the entire portfolio and **leading** FOM_g **and** FOM_{gd}.

Enhanced Safe-Operating Area

3 Safe operating area
I_D=f(V_{DS}); T_C=25 °C; D=0
parameter: t_p



The **SOA** is a diagram defined by the **voltage** and **current conditions** over which a MOSFET can be **operated without incurring into permanent damage or degradation**.

The comparison between SOAs for 80V Best-in-Class OptiMOS™ 5 (1.9 mΩ) and OptiMOS™ 6 (1.8 mΩ) products in PQFN 5x6 mm², highlights a **remarkable improvement in the linear region of operation.**

Application results: hard- and soft-switching DC/DC intermediate bus converters

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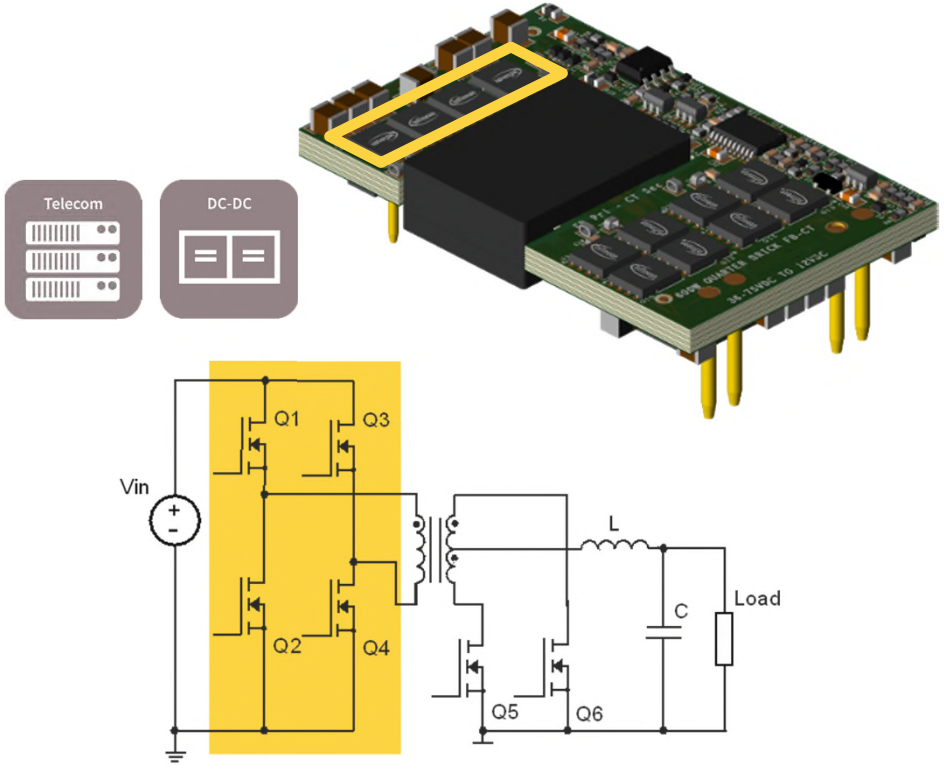
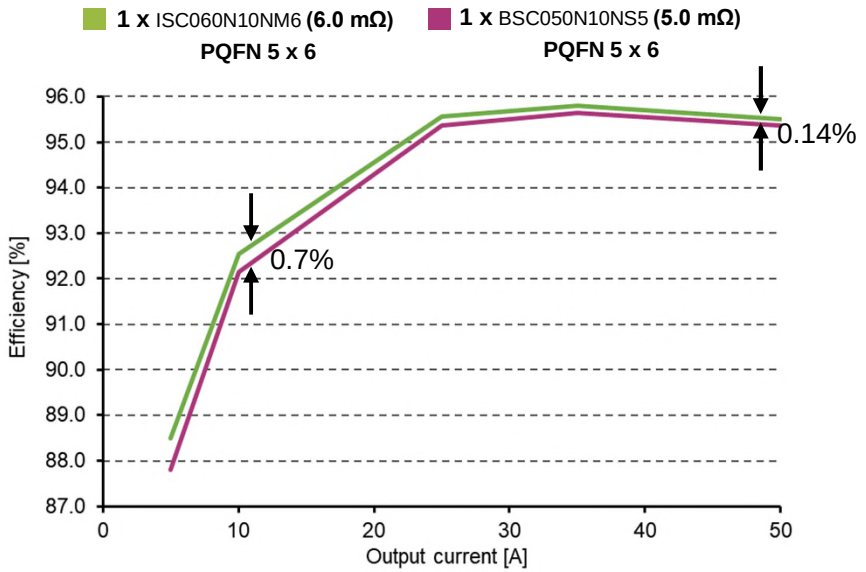
100 V: 600 W Intermediate Bus Converter for Telecom- Primary Side – Hard Switching

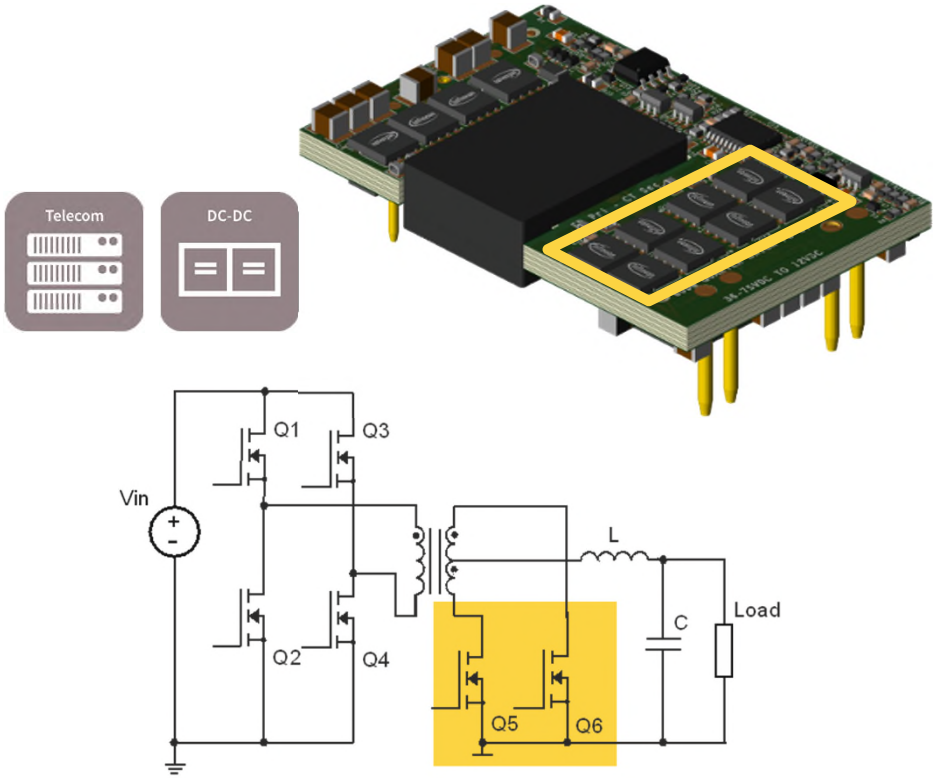


Primary Side Efficiency @ 48 V DC input

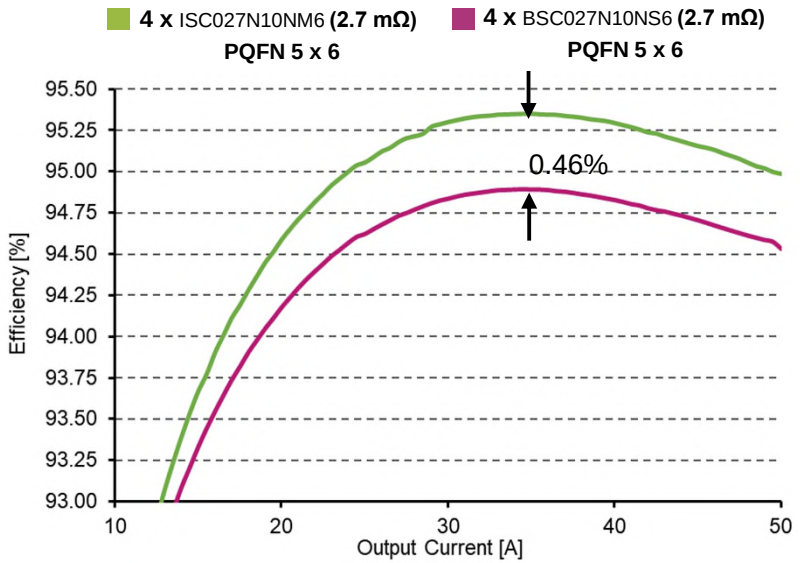


OptiMOS™ 6 – 100 V ISC060N10NM6 (6.0 mΩ) **in PQFN 5x6 package** outperforms OptiMOS™ 5 for comparable $R_{DS(on)}$, thanks to superior switching performances. **Mid- to full-load efficiency improves** thanks to lower R_g and Q_{gd}.

100 V: 600 W Intermediate Bus Converter for Telecom- Secondary Side – Soft Switching



Secondary Side Efficiency @ 53 V DC input



OptiMOS™ 6 – 100 V ISC027N08NM6 (2.7 mΩ) **in PQFN 5x6 package** outperforms OptiMOS™ 5 for same $R_{DS(on)}$. **Light-load efficiency improves** thanks due to lower Q_g, **mid- to full-load efficiency improves** thanks to lower Q_{RR}.

80 V: 1 kW LLC Intermediate Bus Converter for Datacenter- Primary Side - Resonant Operation 300 kHz

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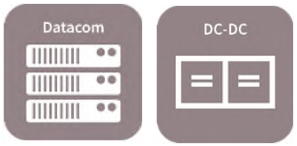
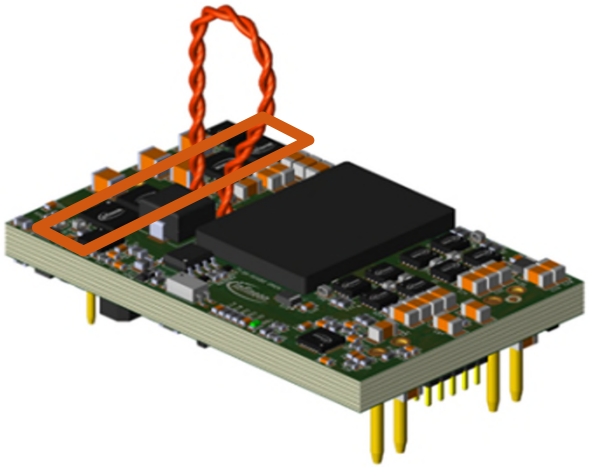
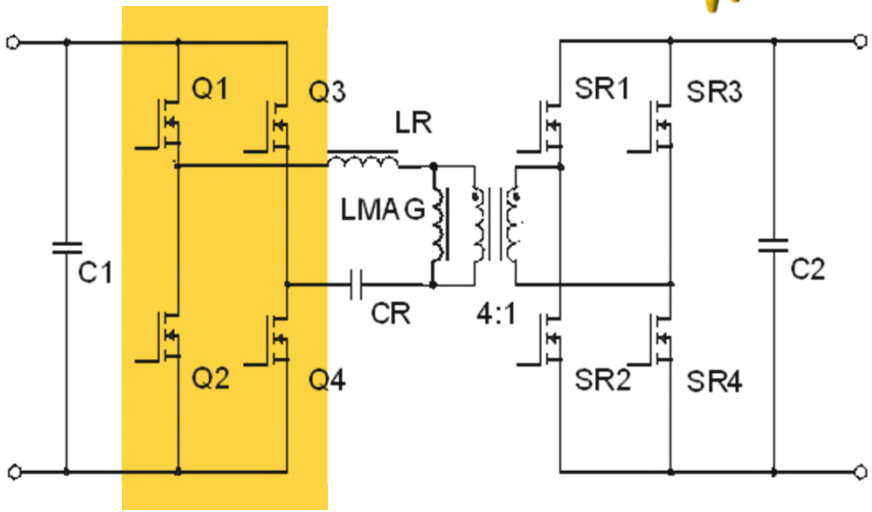
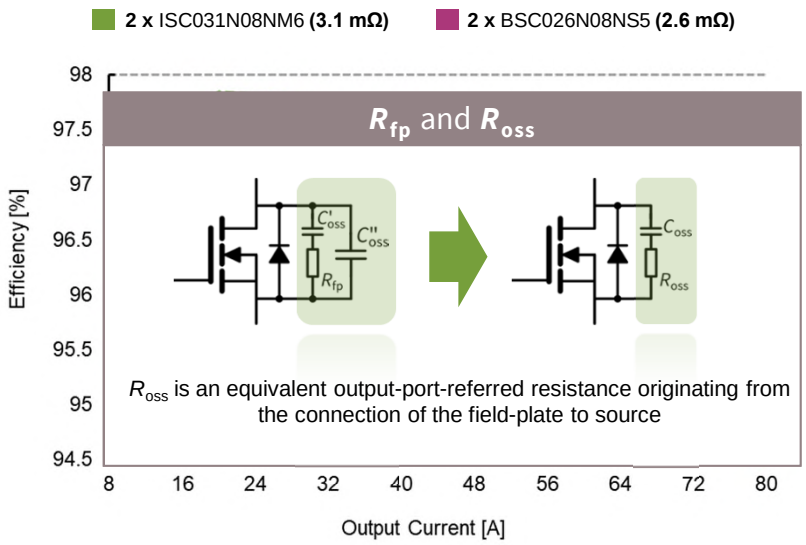






Efficiency @ 44 & 48 V DC input



OptiMOS™ 6 80 V ISC031N08NM6 (3.1 mΩ) in **PQFN 5x6 package** outperforms OptiMOS™ 5 for comparable $R_{DS(on)}$. **Efficiency improves up to 0.7%**, thanks to improvements in Q_g and R_{oss}. Potential to replace two devices by one BiC.

Conclusion

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Conclusion

– A new power MOSFET technology was developed that improves all important device parameters

– The substantial gain in the device performance is enabled on technology level by the use of a unique 3D charge compensation approach, with better utilization of the silicon area and the first time use of a metal gate in a trench power MOSFET

– The lowered charges together with the improved switching homogeneity enhance the system efficiency in the application across all load conditions

– Optimized transfer characteristics with a low temperature coefficient enable a safe operating area that is enhanced over the capabilities of the predecessor technology, widening the range of suitable applications

– Efficiency measurements in targeted SMPS (switched mode power supply) applications under hard- and soft-switching conditions confirm the promises from the findings on the semiconductor device level, with realized efficiency improvements of up to 0.7 %

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